

FIG. 1

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4 6 - 3

4 6

RSSI SIGNAL

REFERENCE VOLTAGE

INPUTTING
AN L + R
COMPONENT SIGNAL

V DD

OUTPUTTING
AN L + R
COMPONENT SIGNAL

5 0 5 0

5 0 5 0

5 0

5 0

4 6 - 2

5 1

S 2

4 6 - 1

F I G. 2

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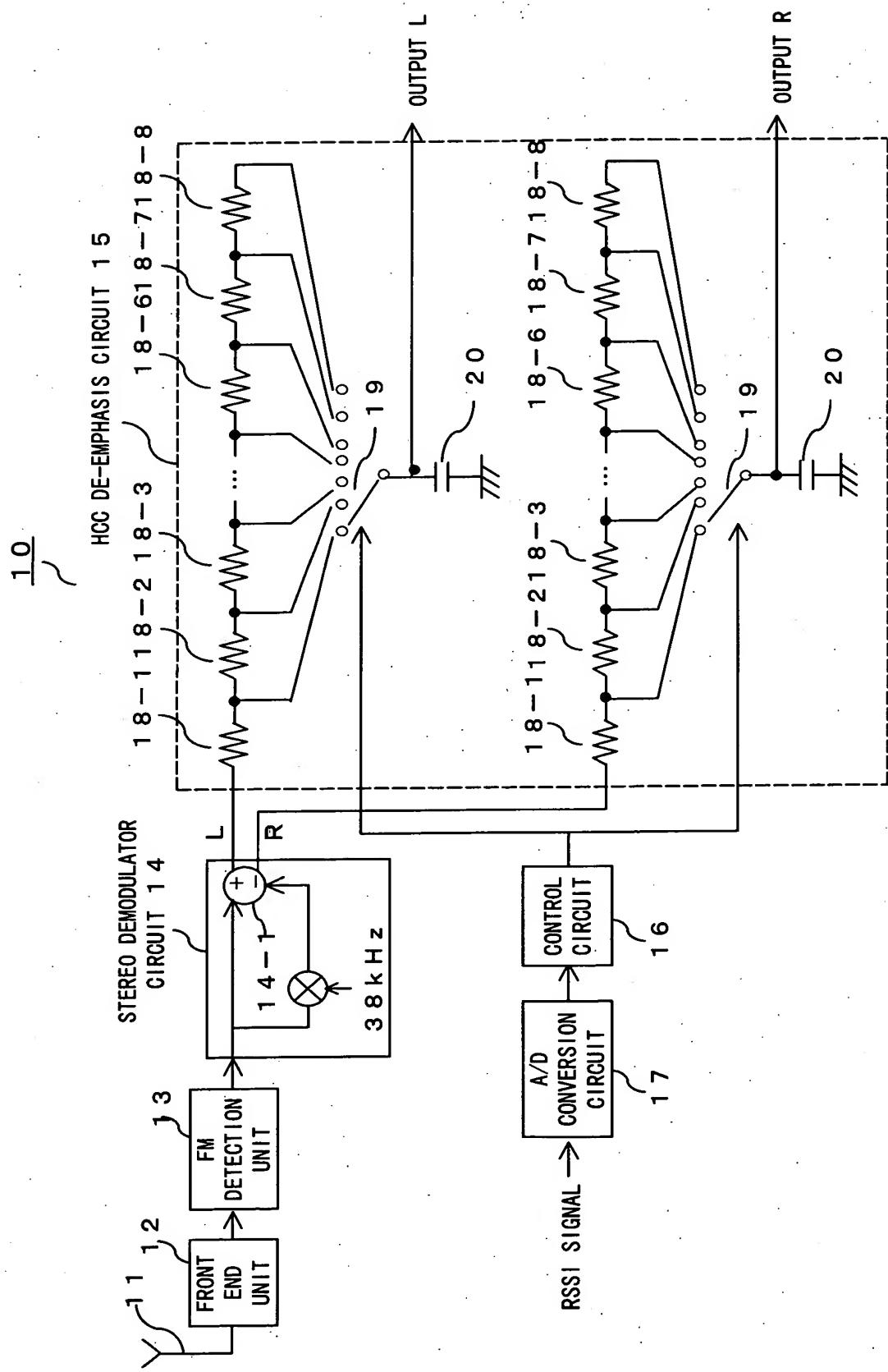


FIG. 3

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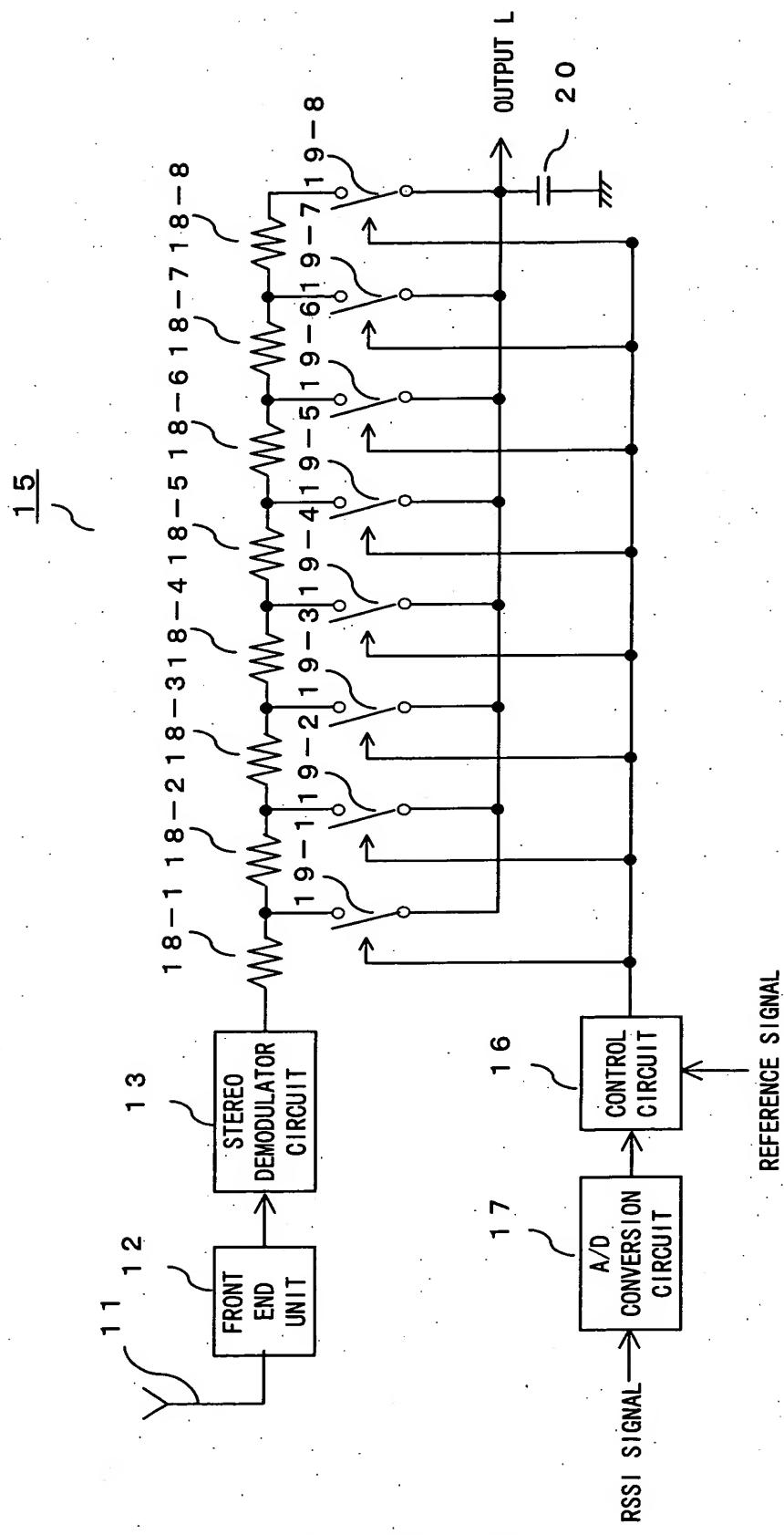


FIG. 4

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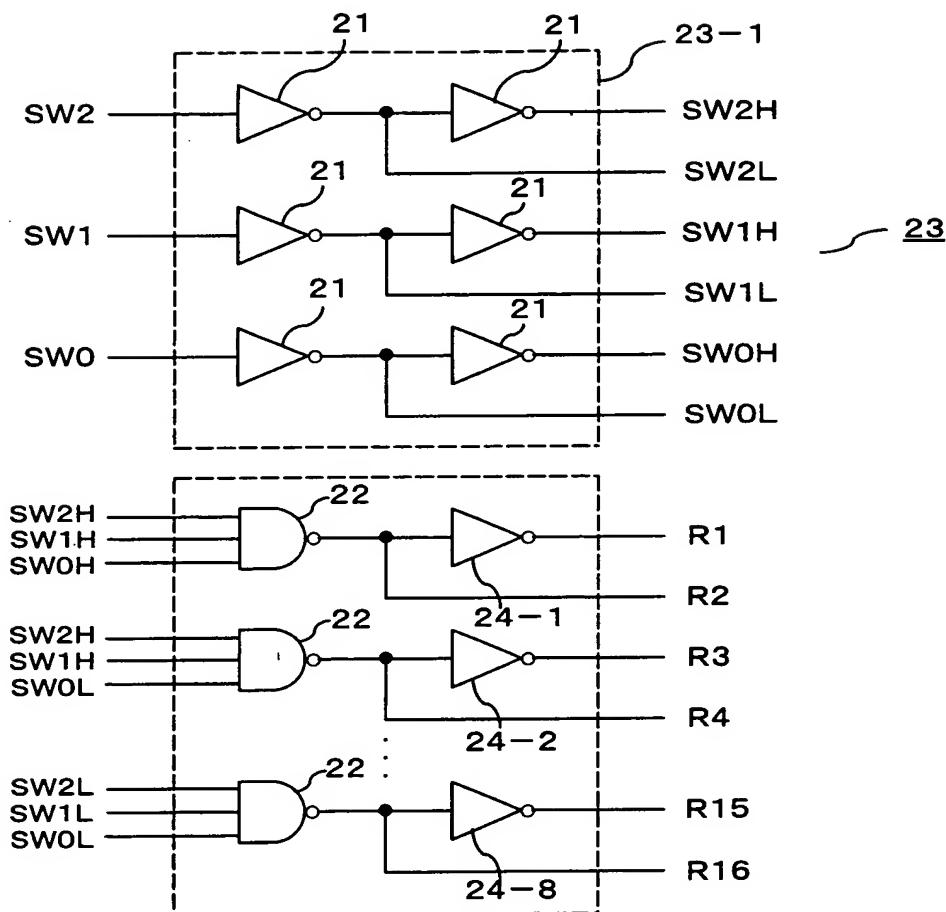


FIG. 5 A

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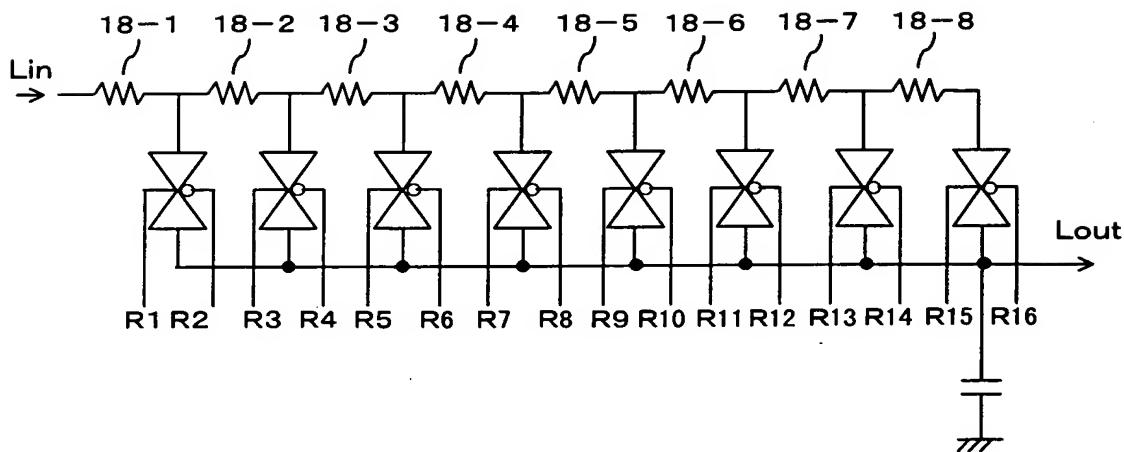


FIG. 5B

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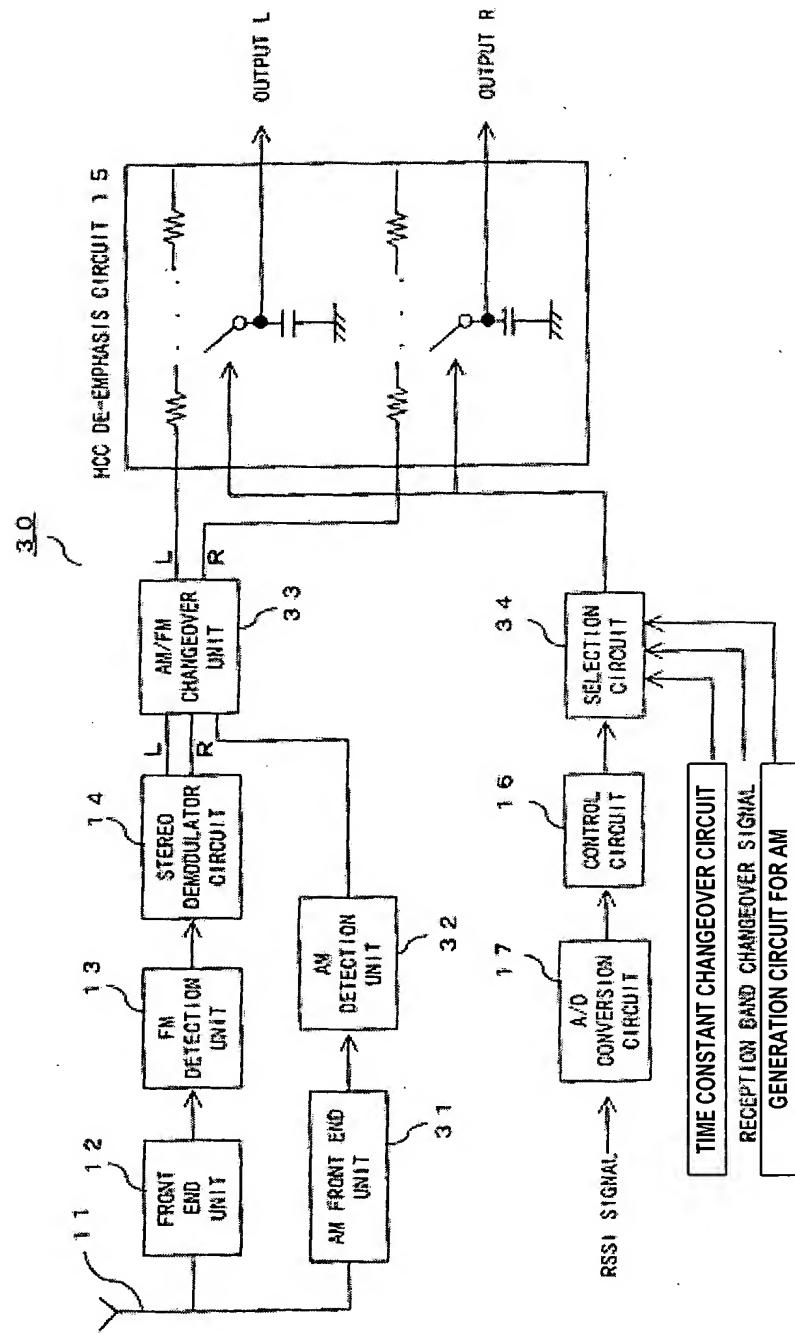
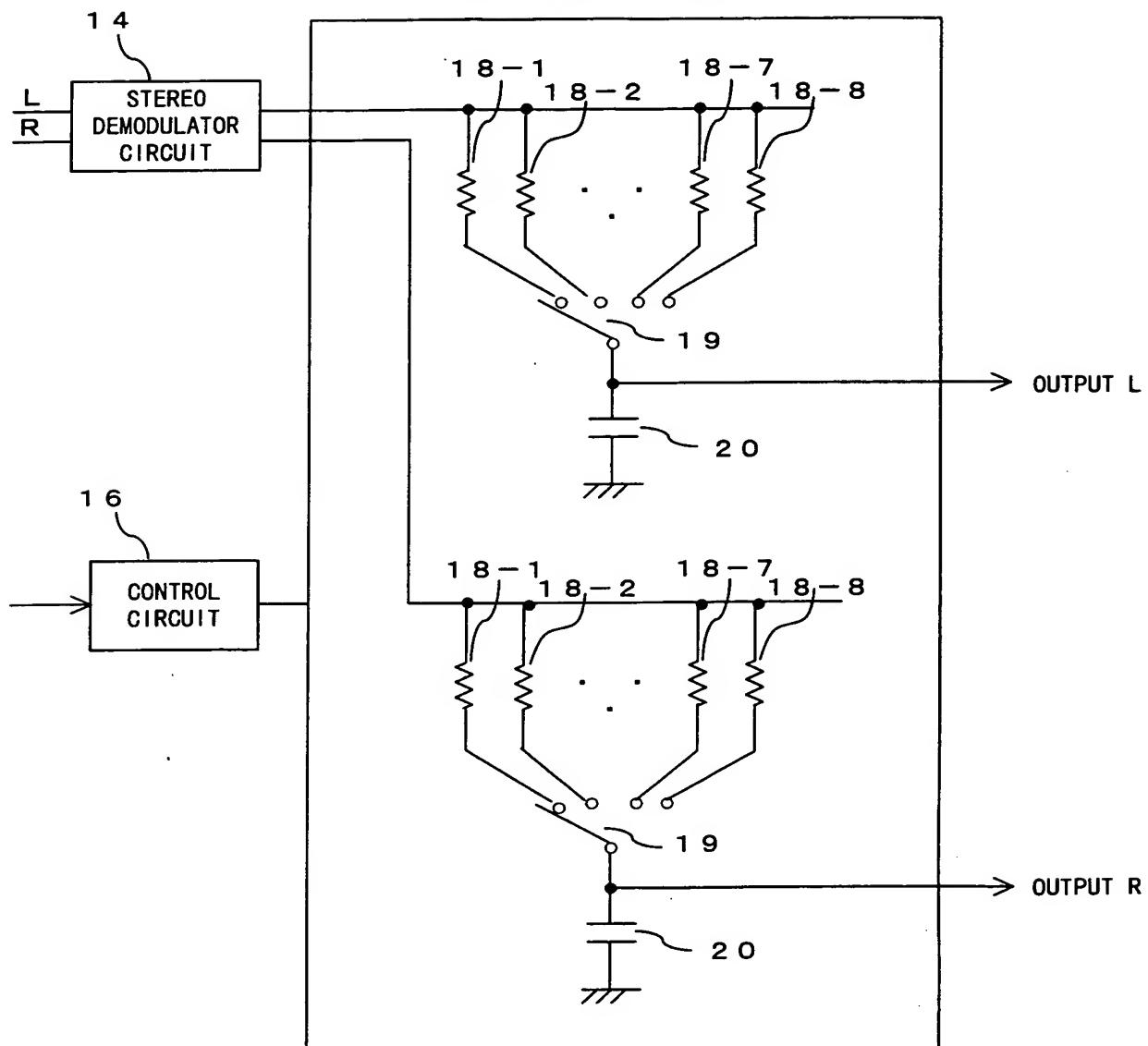


FIG. 6

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HCC DE-EMPHASIS CIRCUIT 35



F I G. 7